

S.No. : 384

BCAT 125

No. of Printed Pages : 05

Following Paper ID and Roll No. to be filled in your Answer Book.

**PAPER ID : 1110**

Roll  
No.

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

## BCA Examination 2018-19

(Even Semester)

### COMPUTER ORGANIZATION AND ARCHITECTURE

*Time : 3 Hours]*

*[Maximum Marks : 100*

**Note :** Attempt all questions.

#### SECTION – A

1. Fill in the blanks. 1 × 10 = 10
- (a) The memory which is read only known as .....
- (b) Full adder is constructed by using .....
- (c) ..... are used to one type of number system to other form.
- (d) ..... is a shift operator.

- (e) Modem stands for .....
- (f) A memory that requires refreshing of data is .....RAM.
- (g) Cache memory works on the principle of .....
- (h) A decoder is used for .....
- (i) MBR is a .....
- (j) Shift register is used for .....

B. State True / False :

- (a) The register that holds a reference for the memory unit is usually called MAR.
- (b) Fixed length, easily decoded instruction format is one of the characteristics of CISC machine.
- (c) The 8085 microprocessor contains 4 different types of flags.
- (d) The memory that directly communicated with CPU is known as primary memory.
- (e) Control bus is a group of wires used for purpose of data flow.

- (f) The Read and write memory is called ROM.
- (g) A command given to computer is called instructions.
- (h) Digital computer are used for counting purpose.
- (i) Assembler is a Hardware device.
- (j) DMA is used for memory access.

### SECTION – B

Note : Attempt any three questions.  $10 \times 3 = 30$

2. (a) What is RISC? Explain with proper example.
- (b) Define cache memory. Explain the mapping process followed in cache memory.
- (c) Describe how DMA is used to transfer data from peripherals.
- (d) Describe Daisy-chaining priority in context to priority interrupt.
- (e) Briefly describe various register sets of CPU. Also discuss the role of Accumulator register.

/ P. T. O.

## SECTION - C

**Note :** Attempt any one from each :  $10 \times 5 = 50$

3. Describe the interaction between hardware and software in a computer system.

OR

Define micro instruction. What are the types of micro instruction available?

4. Explain the fetch and execution cycle in detail by giving an example.

OR

Define the term instruction format. What are three address instruction? Show how statement  $Z = (A - B) / (C + D)$  will be implemented by stack.

5. Explain the different data schemes. Also explain the I/O bus and its bus interface module.

OR

Write notes on I/O processor and I/O Channel.

6. What is virtual memory? Why is necessary to implement virtual memory? Explain the virtual memory address translation.

OR

- Explain the various types of secondary storage devices.
7. Discuss six segment pipelining. Explain Architecture pipeline in details. Also discuss pipeline conflicts.

OR

Write short note on the following :

- (i) SISD
- (ii) MIMD
- (iii) Data Hazards
- (iv) CISC.

\*\*\*